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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/703,034	10/31/2000	Joseph R. Zbiciak	TI-30553	8913

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EXAMINER	
DO, CHAT C	

ART UNIT	PAPER NUMBER
2193	

DATE MAILED: 03/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/703,034	ZBICIAK, JOSEPH R.	
	Examiner	Art Unit	
	Chat C. Do	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4,5,9-11,13,16 and 17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4,5,9-11,13,16 and 17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is responsive to Appeal Brief filed 12/21/2005.

2. Claims 1, 4-5, 9-11, 13, and 16-17 are pending in this application. Claims 1 and 13 are independent claims. This Office Action is made non-final.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 4-5, 10-11, and 13 are rejected under 35 U.S.C. 103(a) as being obvious over Saishi et al. (U.S. 6,167,419) in view of Pitsianis et al. (U.S. Patent Application Publication No. 2003/00088601).

Re claim 1, Saishi et al. disclose in Figures 5-9 a method of performing a product operation with rounding and shifting in a microprocessor in response to a single rounding product instruction (e.g. abstract and columns 2-4), the method comprising the steps of: fetching a first pair of elements (e.g. Figure 5 501 and 502 as multiplier and multiplicand); forming a first product of the first pair of elements (e.g. output of 509); and rounding the combined product to form an intermediate result via an arithmetic circuit having a first input receiving first product, and a carry input to a mid-position

receiving rounding value to form the intermediate result (e.g. 803, 806, and 807 in Figure 8 and col. 8 lines 11-63); and right shifting the intermediate result a selected amount to form a final result (e.g. Figure 8 with 809 right shift step). Saishi et al. fail to disclose the operation is dot product operation with first and second pair elements as input elements by combining the products of first and second pair of elements. However, the dot product operation is well known in the art as seen in Pitsianis et al.'s Figures 3B and 6 wherein it discloses the fetching a first pair of elements (e.g. Xr and Yi in 603 and 605) and a second pair of elements (e.g. Xi and Yr in 603 and 605); forming a first product (e.g. 617) of the first pair of elements and a second product (e.g. 619) of the second pair of elements; combining (e.g. 625) the first product with the second product; form a combined product (e.g. output of 625) and rounding (e.g. 627) the combined product to form an intermediate result via an arithmetic circuit (e.g. 627) having a first input receiving said first product, a second input receiving said second product. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add a dot product operation as seen in Pitsianis et al.'s invention into Saishi et al.'s invention because it would enable to efficiently compute the sum of products which would be used in many practical applications (e.g. FFT).

Re claim 4, Saishi et al. disclose in Figures 5-9 the rounding value is 2n and the selected shift amount is n+l (e.g. Figure 8 wherein n = m and 805 at m+1).

Re claim 5, Saishi et al. disclose in Figures 5-9 n has a fixed value of fifteen (e.g. m = 15).

Re claim 10, Saishi et al. disclose in Figures 5-9 the step of combining comprises subtracting the product of second pair of elements from the product of first pair of elements (e.g. 306 as subtractor).

Re claim 11, Saishi et al. disclose in Figures 5-9 the step of combining comprises adding the product of second pair of elements to the product of first pair of elements (e.g. 306).

Re claim 13, it is a system claim of claim 1. Thus, claim 13 is also rejected under the same rationale as cited in the rejection of rejected claim 1.

5. Claim 9 is rejected under 35 U.S.C. 103(a) as being obvious over Saishi et al. (U.S. 6,167,419) in view of Pitsianis et al. (U.S. Patent Application Publication No. 2003/00088601) as applied to claim 1 above, and further in view of Slavenburg et al. (U.S. 5,963,744).

Re claim 9, Saishi et al. in view of Pitsianis et al. do not disclose the steps of forming the first product and forming the second product treats a one of the first pair of elements as a signed number value and treats another one of the first pair of elements as an unsigned number value. However, Slavenburg et al. disclose in Figure 18 a dot product wherein the steps of forming the first product (e.g. first element of rsrc2 and rsrc1) and forming the second product (e.g. second element of rsrc2 and rsrc1) treats a one of the first pair of elements as a signed number value (e.g. rsrc2) and treats another one of the first pair of elements as an unsigned number value (e.g. rsrc1). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the steps of forming the first product and forming the second

product treats a one of the first pair of elements as a signed number value and treats another one of the first pair of elements as an unsigned number value as seen in Slavenburg et al.'s invention into the combined invention of Pitsianis et al. in view of Adelman et al. because it would enable to increase the flexibility of the system by handling multiple formatted operand registers (e.g. col. 2 lines 65-67).

6. Claims 16-17 are rejected under 35 U.S.C. 103(a) as being obvious over Saishi et al. (U.S. 6,167,419) in view of Pitsianis et al. (U.S. Patent Application Publication No. 2003/00088601) as applied to claims 1 and 13 respectively above, and further in view of Greggain et al. (U.S. 5,559,905).

Re claim 16, Saishi et al. in view of Pitsianis et al. fail to disclose the step of shifting further includes sign extending the intermediate result. However, Greggain et al. disclose in Figure 4 the step of shifting further includes sign extending the intermediate result (e.g. Figure 4 part 51 and 49 and col. 4 lines 15-33). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the sign extending in shifting step as seen in Greggain et al.'s invention into Saishi et al. in view of Pitsianis et al.'s invention because it would enable to restore the significance of the product values being produced (e.g. col. 4 lines 15-33).

Re claim 17, it is a system claim of claim 16. Thus, claim 17 is also rejected under the same rationale as cited in the rejection of rejected claim 16.

Response to Arguments

7. Applicant's arguments with respect to claims 1, 4-5, 9-11, 13, and 16-17 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. U.S. Patent No. 6,957,244 to Jou et al. disclose a reduced-width low-error multiplier.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (571) 272-3721. The examiner can normally be reached on M => F from 7:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaki Kakali can be reached on (571) 272-3719. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do

Examiner
Art Unit 2193

February 28, 2006

KAKALI CHAKI
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100